THAT WHICH IS CLAIMED IS:

1. A switching circuit for switching an output signal (CKS) to one of a plurality of N input clock signals (CK1-CKN) which are delayed relative to one another, in response to a control (CNT), characterized in that it comprises circuit means (31-316, 7) responding to the control (CNT) in order to enable the transmission, on the output signal (CKS), of a new signal (CK(i-1); CKi) of the plurality of input signals which is advanced or delayed relative to a current signal (CKi; CK(i-1)) of the plurality of input signals which is currently transmitted on the output signal (CKS), the circuit means (31-316, 7) enabling the transmission of the new signal (CK(i-1); CKi) before disabling the transmission of the current signal (CKi; CK(i-1)) on the output signal (CKS) so as to prevent the production of false signals during the switching of the output signal from one of the clock signals to another.

2. A switching circuit according to Claim 1, characterized in that the circuit means (31-316, 7) comprise a plurality of N circuit blocks (31-316) each of which receives a respective clock signal (CK1-CK16) of the plurality of N signals and can be selected to supply the respective signal (CK1-CK16) to its own output (EN_CK1-EN_CK16) which is operatively connected to the output (CKS) of the switching circuit, the circuit blocks being operatively connected to one another to form a ring and each circuit block generating a disabling signal (K1-K16) to be supplied to the circuit blocks adjacent to it in the ring, the

disabling signal being activated when the circuit block is selected in order to disable the respective outputs EN_CK1-EN_CK16) in the adjacent blocks.

3. A switching circuit according to Claim 2, characterized in that the disabling signal (K1-K16) is activated after the output (EN_CK1-EN_CK16) of the respective circuit block has been enabled to provide the respective local clock signal (CK1-CK16).

4. A switching circuit according to Claim 3, characterized in that it comprises a decoding circuit (6) for decoding control signals (CNT) for the switching circuit, the decoding circuit (6) activating one of N selection signals (S1-S16) for the circuit blocks (31-316), in dependence on a state of the control signals (CNT).

5. A switching circuit according to Claim 4, characterized in that all of the clock signals (CK1-CKN) have the same period T.

6. A switching circuit according to Claim 5, characterized in that the clock signals (CK1-CKN) are delayed equally relative to one another by a fraction T/N of the period T.

7. A switching circuit according to Claim 6, characterized in that each of the circuit blocks (31-316) comprises first circuit means (FF3, I1, A2, FF5, FF6) for generating a pulse on the disabling signal (K1-K16) as a result of the activation of the respective selection signal (S1-S16).

8. A switching circuit according to Claim 7, characterized in that each of the circuit blocks (31-316) comprises second circuit means (FF3, FF4, A2, O1, I1, A2, O2, A3, FF7) for activating a signal (ENi) for enabling the transmission of the respective local clock signal (CK1-CKN) in response to the activation of the respective selection signal (S1-S16), the enabling signal (ENi) being activated in synchronism with the respective local clock signal (CK1-CKN).

9. A switching circuit according to Claim 8, characterized in that the second circuit means (FF3, FF4, A1, O1, I1, A2, O2, A3, FF7) receive the disabling signals (K1-K16) from the adjacent circuit blocks (31-316) and deactivate the enabling signal (ENi) when one of the disabling signals is activated.

10. A circuit for recovering data in a serial data flow comprising a generator (4) generating a plurality of N clock signals (CK1-CKN) of equal period T which are delayed equally relative to one another by a fraction T/N of the period T, the generator (4) supplying a switching circuit (3) for switching an output (CKS) to one of the clock signals (CK1-CKN), the output (CKS) being supplied to a phase comparator (1), together with a signal (BK) carrying a flow of data being received, and control means (5) for the switching circuit (3), the control means (5) receiving from the phase comparator (1) signals (+/-) indicative of the phase difference between the output (CKS) of the switching circuit (3) and the flow of data being received (BK) and consequently controlling the

switching circuit (3) so as to switch the output (CKS) to a clock signal (CK1-CKN) with a smaller phase difference, characterized in that the switching circuit is in accordance with any one of the preceding claims.

11. A circuit according to Claim 10, in which the generator (4) is a delay-locked loop circuit (DLL).

12. A circuit according to Claim 10, in which the signal (BK) carrying the flow of data received and the output (CKS) of the switching circuit (3) are supplied to data sampling circuit means (2), the output (CKS) of the switching circuit acting as a synchronizing signal for the sampling.

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